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"DEVELOPMENT OF THIN WRAPAROUND JUNCTION SILICON SOLAR CELLS"

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16. Abstract

The objective of this contract was to apply state-of-the art technologies to fabricate 50um thick 2X4cm, coplanar back contact (CBC) solar cells with AMO efficiency above 12 percent, with a goal of 14 percent. An additional requirement was that the cells have low solar absorptance. A wraparound junction (WAJ) with wraparound metallization was chosen to meet the contract goal because of its proven capability for good quality thin cells. This WAJ approach seemed best suited to adaptation to 50um cells, since it avoided the need for very complex fixturing, especially during rotation of the cells for providing adequate contacts over dielectric edge layers. The WAJ method eased the requirements that the contact metal continue around the thin fragile slice edge. In addition, the contact adhesion to silicon rather than to an insulator was considered to be better. Also, the higher conductivity of the WAJ favored use of electroplating to build up the WA edge contacts. Preliminary WAJ cells made with this method had fill factors as high as 0.75. This was a good indication that shunt resistance caused by poor WAJ diode quality, and series resistance from the WA contact, could be controlled to give good cell performance.

The cells developed reached 14 percent AMO efficiency (at 25°C), with solar absorptance values of 0.73. In addition to regular state-of-the-art deliveries, fifty cells were delivered from a final run, using the best procedure developed. These cells all had efficiency above 12 percent, with an average efficiency of 13.0 percent . Important space-cell environmental tests were performed on these cells and the thin CBC cells performed well.

The optimized design configuration and process sequence were used to make fifty (50) deliverable CBC cells. These cells were all above 12 percent efficiency and had an average efficiency of ~ 13 percent, with the best cell efficiency of 14.1 percent (at 25°C). The overall yield with efficiency >12 percent was 37 percent, with the best yield of 41 percent. The solar absorptance value was 0.73.

Also, results of environmental tests (humidity-temperature, thermal shock, and contact adherence) performed in accordance with typical space-cell specifications are given.

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ABSTRACT

During this contract, current advanced technologies for fabricating high efficiency, low solar absorptance, thin (~50um) silicon solar cells were adapted to provide the cells with coplanar back contacts (CBC). This involved use of a wrapped-around PN junction, and modification of the contact mask design and application of these masks.

The cells developed reached 14% AMO efficiency (at 25°C), with solar absorptance values of 0.73. In addition to regular state-of-the-art deliveries, fifty cells were delivered from a final run, using the best procedure developed. These cells all had efficiency above 12%, with an average efficiency of 13.0%. Important space-cell environmental tests were performed on these cells and the thin CBC cells performed well.

SUMMARY

The objective of this contract was to apply state-of-the-art technologies to fabricate 50um thick, 2x4cm, coplanar back contact (CBC) solar cells with AMO efficiency above 12%, with a goal of 14%. An additional requirement was that the cells have low solar absorptance (α_s). A wraparound junction with wraparound metallization was chosen to meet the contract goal.

During the period of this contract, major effort was successfully directed toward the improvement of thin cell efficiency and optimizing process steps, to combine both advanced thin cell technologies and CBC cell design. The report describes the cell design features which required optimization to meet the goals, and also details the various process steps which were used to make the cells.

The optimized design configuration and process sequence were used to make fifty (50) deliverable CBC cells. These cells were all above 12% efficiency and had an average efficiency of ~13%, with the best cell efficiency of 14.1%. The overall yield with efficiency >12% was 37%, with the best yield of 41%.

The photovoltaic data and yield experience for these fifty cells is included. Also, given are the results of several key environmental tests (humidity-temperature, thermal shock, and contact adherence) performed in accordance with typical space-cell specifications.

With a background of proven requirements for good quality thin cells, the decision was made to follow the wrapped around junction (WAJ) approach in this contract. This WAJ approach seemed best suited to adaptation to 50um cells, since it avoided the need for very complex fixturing, especially during rotation of the cells for providing

adequate contacts over dielectric edge layers. The WAJ method eased the requirements on the contact continued around the thin fragile slice edge and the contact adhesion to silicon rather than to an insulator was considered to be better. Also, the higher conductivity of the WAJ was in favor of use of electroplating to build up the WA edge contacts. We had made preliminary WAJ cells with this method and had seen fill factors as high as 0.75, a good indication that shunt resistance caused by possible poor WAJ diode quality, and series resistance from the WA contact, could be controlled to give good cell performance.

With this background, we now proceed to describe the technical details of the contract work.

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1.0 INTRODUCTION

1.1 Background

High efficiency, thin silicon cells (~50um thick) had been developed to give efficiencies close to those obtainable on thicker cells (15% for textured surfaces, 14% for untextured surfaces), and had shown improved radiation tolerance and increased power-to-weight ratio over thicker cells. Solar cells with coplanar back contacts (CBC), i.e. with contacts to both N+ and P+ regions at the back surface, have advantages over conventional solar cells in the chance of simpler interconnection, leading to reduced array assembly costs, improved reliability, and simpler coverglass application, along with possible increase in active area and efficiency.

In the past few years, a suitable process sequence and proper handling methods had been developed at Applied Solar Energy Corporation to make 50um thick solar cells with good yields, although the throughput rates were lower than for thicker cells. This process technology was adapted to provide coplanar back contacts. Several techniques for providing CBC's have been tried since the earliest Bell Laboratories cells. These techniques were:

i) Wrapped-around junction (references 1, 2) wherein the front diffused layer was continued around the end(s) onto the back surface, and suitably isolated contacts were applied to the P and N regions on the back. This design had shown reduced diode quality, ascribed to the poor quality of the edge junction. Also the back contact was reduced, and the increased series resistance lowered cell output. The reduced back contact area decreased the effectiveness of back surface field (BSF) or a back surface reflector (BSR).

ii) Wrapped-around contacts (references 3 and 4) where an insulating layer is deposited around the cell edge(s) and onto part of the back surface, and the front surface contact is continued around this insulating layer. Typical insulating layers used were discrete tapes, deposited dielectrics, or screen-printed glassy layers. These latter layers were successful for thicker cells (10 mils) (reference), but gave serious difficulties when the silicon slice was ≤4 mils. Use of thin evaporated or CVD layers had been promising, although they involved some retreat from the original concept (reference 5) where the insulating layers were deposited over a back contact which covered the whole back surface area; the modification used most involved no back contact in the wrapped-around contact areas, to allow the dielectric layer to be deposited directly on the bulk silicon.

iii) Interdigitated back contact cells (references 5 and 6). These cells have demonstrated efficiencies above 12%, (reported as high as 14%), but involve fairly complex process steps. Also, because of their reduced tolerance to radiation, this design was ruled out for this contract.

iv) Alloyed through contacts. Deeply penetrating alloying methods, especially thermomigration have been suggested to provide CBC, but the quality of the main junction was reported to be poor.

v) Etch through structures. Structures with single holes in the silicon had shown defects similar to those observed on the first two methods. Use of multiple holes, e.g. in polka dot cells (reference 7) involve some loss of mechanical integrity of the cell, and also include the complexity of interdigitated contacts.

After careful consideration of the scope and limitations of current process methods used to make high efficiency thin cells, the best CBC thin cell method was

considered to be a modified WAJ method. This is because the WAJ method eases the requirements on the contact continued around the thin fragile slice edge, and eliminates the need for very complex fixturing, especially during rotation of the cells. It is easier to provide adequate contacts and reduce the need for an insulating layer with minimum stress on the edges. Also, the contact adhesion to silicon rather than to an insulator was considered to be better.

At the time the contract started, we had made preliminary CBC cells using this method and had shown cell efficiency of 12% with fill factor as high as 75%. With this background, we were directed, under this contract, to optimize the process sequence and parameters for producing thin WAJ solar cells toward a goal of 14% AMO efficiency, with additional constraint to keep the α's low.

1.2 General Approach and Baseline Cell Design

Several design factors for WAJ thin cells are the same as those required for conventional thin cells. These factors must be optimized and integrated with the additional steps to demonstrate a complete sequence to form high efficiency WAJ thin cells. Briefly the optimization involves:

a) Choice of silicon of suitable resistivity and minority carrier diffusion length (L).

b) Careful thinning to provide plane slices.

c) (Optional) good texture finish.

d) Formation of highly doped "like" layer (P+/P for this contract which required N+PP+ cells) which gave good BSF properties (enhanced Isc and Voc), while not adding serious stress in silicon, or the chance of severely reduced L. In addition, this BSF layer should allow high back surface reflectance to be obtained.

e) Shallow N+ layer (~0.2um).

f) Design and formation of a grid contact configuration which provided good coverage via close spaced narrow lines, with good line conductance.

g) A suitable back contact, which gave low ohmic contact, combined with BSR properties, and did not involve appreciable stress.

h) Optimized AR coating.

The contact areas to the N+ and P+ regions must be readily bonded by welding or soldering. In addition the overall cell properties must be compliant with advanced space cell needs, and must also retain all necessary environmental performance.

Most important, these optimized steps must be capable of combination with handling and fixturing methods which give favorable yields for the thin slices.

2.0 TECHNICAL FEATURES

2.1 Initial Process Sequence

The process sequence which had demonstrated CBC cell performance up to 12%, is given in Table 1, and the following comments amplify the details given in the Table.

Step 1

There are a few restrictions on the silicon which can be used. Resistivity in the range 2 to 15 ohm-cm can be used, with 10 ohm-cm being the most likely value. For ease of etching (and to allow for possible texturing), (100) oriented slices were used. Care in slice preparation before etch-thinning led to more uniform thin slices, with less breakage. A 3" slice able to give three 2x4cm cells is processed.

Step 2

A good quality SiO_2 layer is deposited on the slice.

Step 3

A back surface window opened-up using a simple mask.

Step 4

A boron diffusion to provide BSF is made through this SiO_2 window. The advantage of this BSF method is that it can provide both an effective BSF and a good BSR surface.

Step 5

After cleaning off SiO_2 and glassy layers, a new SiO_2 layer is deposited on the major surface (using a CVD process).

Step 6

Simple masks are used to provide the N+ diffusion around the wrap around edge, and on the front surface.

Step 7

After cleaning excess SiO_2 and glasses, the front contact is evaporated, using photoresist process to provide the grid pattern.

TABLE I

COPLANAR BACK CONTACT CELL PROCESSING SEQUENCE

STEP	PROCESS
1.	Etch Thin Silicon Slices (to 50um)
2.	SiO_2 Deposition (CVD)
3.	Open Window For BSF Diffusion
4.	Boron Diffusion (BSF)
5.	SiO_2 Deposition
6.	Open Window For N+ Diffusion
7.	Front Contact Formation
8.	Back Contact Formation
9.	AR
10.	Test

Step 8

Using a simple shadow mask, the back surface contact is evaporated.

Step 9

A good quality AR coating is applied to the front surface.

Step 10

The slice processed through the above sequence is larger than the required size. The contact masks provide on this larger slice a number of cells of the required size (typically 6-2x2cm cells or 3-2x4cm cells are obtained per slice). The cells are cut from the processed slice, and tested. Thus the process already provides experience in processing larger area thin slices, suited for larger arrays.

In general, the sequence selected is similar to those which apply present space-cell manufacturing methods to provide high efficiency 50um cells with good yields. The WAJ cell configuration is shown in Figure 1.

Experience in performing the steps given above led to the identification of the key areas which needed modification in order to meet the contract goals.

2.2 Key Process Modifications and Design Parameters

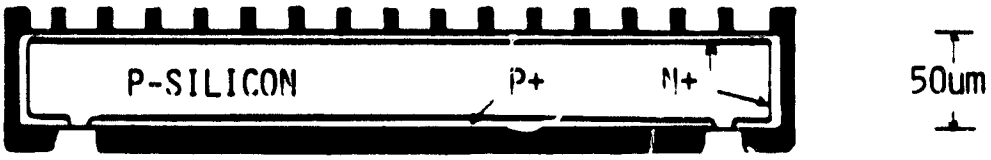
2.2.1 Control Cells

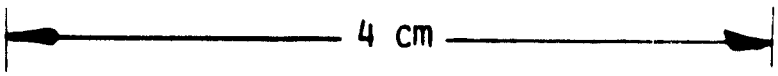
While the key processes were being optimized, it was found useful to process control cells alongside the CBC cells. These control cells were subjected to the same process steps, (were processed as 50um thick, etc.), adjusted not to produce a WAJ structure, but leading to a conventional cell structure with N+ layer (and grid contacts) on the top surface, and the P+ BSF layer and BSR contact structure covering the whole bottom surface. Because many of the optimizing tests involved fairly small differences, the control cells were useful to indicate possible

FIGURE 1

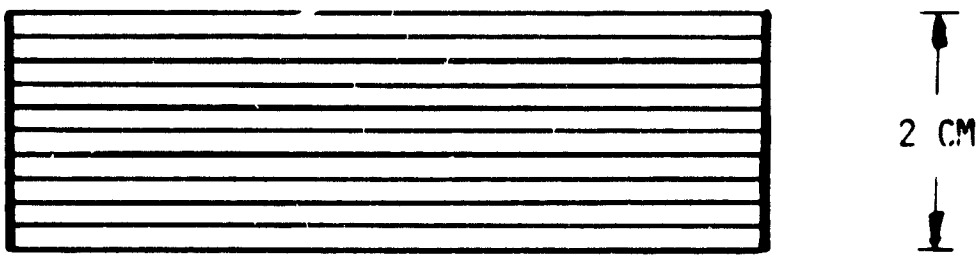
2 MIL COPLANAR BACK CONTACTS CELL (WAJ)

CROSS-SECTIONAL VIEW

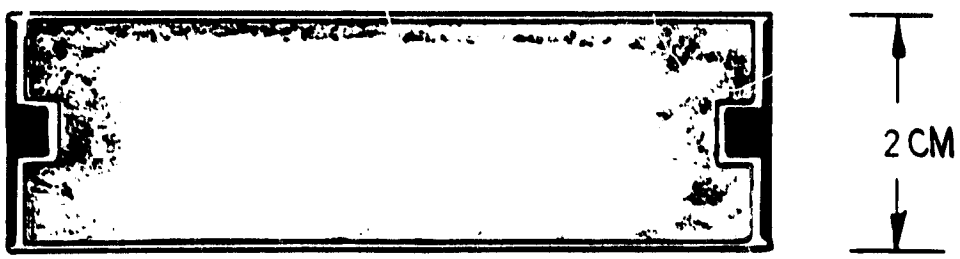




FRONT VIEW



BACK VIEW



interactions of the processes with the silicon, and aided identification of specific effects of the steps needed to provide the CBC structure. Another useful function of the control cells was to indicate the upper limit expected for the CBC cells. Based on such comparisons, we estimated that 13.8% would be the maximum efficiency achievable in the final run; however, based on the best values observed for the individual photovoltaic parameters, it was felt that in a run of one hundred or more cells (to obtain fifty deliverable cells) chance coincidence of these maximum parameters would exceed 14%. As seen in Section 2.8.2 below, this was the case, although as predicted from the control cell limits, the number of such cells was very small.

2.2.2 Oxidation Layer

At an early stage of this contract, the baseline process sequence (see Table 1) was used to make 12% AMO CBC solar cells. These cells had CFF of ~75%, and showing a slight shunting problem. We suspected that the cause of the shunting was pin holes in the CVD silicon dioxide layer resulting in contamination of both N+ and P+ areas.

Later, a decision was made to use thermal oxidation process to replace the chemical vapor deposition (CVD) technique. The thermally grown oxide layer was formed in a steam ambient at 950°C for 5 hours. The CBC cells were completed and tested consequently. The results were shown in Table 2. This result showed that Jsc value was unexpectedly low (typical value are 35mA/cm^2); this low Jsc also led to low Voc (480mV compared to 600mV). The cause of such low Jsc was traced to reduced diffusion length; values of 30um were measured, compared to 150um normally. This was severe degradation of wafer properties most likely was caused by the severe oxidation cycle.

TABLE 2

CELL PERFORMANCE USING THERMAL GROWN SiO_2 LAYER (950°C) AS DIFFUSION MASK

	Voc (mV)	Jsc (mA/cm^2)	CFF (%)	EFF (%)
CBC-3-1	486	25.8	77	7.1
Control Cell	472	25.6	76	6.8

A relaxed oxidation schedule which combined CVD plus low temperature (800°C) densification was used, and this change significantly improved the cell performance. The results are shown in Table 3.

TABLE 3

CELL PERFORMANCE USING CVD PLUS DENSIFICATION SiO_2 LAYER AS DIFFUSION MASK

	Voc (mV)	Jsc (mA/cm^2)	CFF (%)	EFF (%)
CBC-4-4	583	35.8	76	11.7
Control Cell	576	35.8	78	11.9

2.2.3 Grid Patterns

One major advantage of CBC solar cells was possibly increased active area by reducing or eliminating the ohmic bar located across the grid lines at the wraparound edges of the front surface. To obtain maximum cell output, a close-spaced narrow gridline pattern to reduce shallow front junction sheet resistance, and a small "pick-up" ohmic bar to ensure good continuity between the grid pattern and the back surface N+ contact area, were used. This front contact design provided good fill factors and yet retained an active area over 95%.

2.2.4 AR Coating

To obtain maximum cell current, the reflectance must be reduced as much as possible. In cases where the surface is textured, combination with most AR coatings leads to reduced reflectance over the response range of the cells.

In this contract, polished surfaces were required to provide low αs. For such surfaces, a multi-layer AR coating, (using two coating oxides of different refractive indices and thicknesses) gave suitably low reflectance. Some small fluctuations (~1%) in Jsc were traced to corresponding variations from run-to-run in the MLAR coating quality.

2.2.5 Tradeoff Between N+ and P+ Regions On The Back Surface

This tradeoff is the most important feature of WAJ cells. Too much N+ area increases junction shunting, decreasing fill factor; too little P+ area increases series resistance, also decreasing fill factor. In earlier cells, the N+ regions occupied about 10% of the back surface, and the P+ region covered just under 90%. For such cells, the fill factors were slightly lower than found for control 50um cells (with similar process steps, but with conventional front and back contacts). In addition, when the CBC cells were illuminated at different regions, the cell performance changed slightly. Table 4 shows measurements made on a 2x4cm CBC cell with N+ areas ~10% of the back surface. When the whole cell area was illuminated, the Jsc was 35.3 mA/cm^2 (the J_r and J_b values show the current densities for AMO illumination either above or below 6000Å). The overall FF was low (0.73). Also, the sum of the Jsc values for the two wavelength ranges, exceeded the total Jsc by 2.5%. If only the center of the cell was illuminated (WAJ ends not illuminated), the FF increased to 0.75, total Jsc increased, and the sum of the separate spectral contributions equalled the total Jsc. If the WAJ ends

only were exposed, Voc decreased slightly, CFF decreased to 0.72, and the difference between the separate Jsc components and the total Jsc was larger (5%). It was also found that physically reducing the N+ areas only (with no increase in the P+ area) increased FF slightly.

TABLE 4

EFFECTS OF NON-UNIFORM ILLUMINATION

	Voc (mV)	Jsc mA/cm^2	Jr mA/cm^2 (λ>6000A)	Jb mA/cm^2 (λ<6000A)	Jb+Jr mA/cm^2	CFF %	$\frac{(Jb+Jr)-Jsc}{Jsc}$
Uncovered	608	35.3	20.5	15.7	36.2	73	2.5%
Covered Two WAJ Ends	590	36.4	20.7	15.6	36.3	75	0.2%
Cover Center Part	583	33.0	19.5	15.2	34.7	72	5.1%

To explore this tradeoff further, masks were used which gave N+ areas 10.2%, 5.1%, and 2.3% respectively; the corresponding P+ areas were 88.5%, 93.6%, and 96.6%. Table 5 shows the photovoltaic properties of cells made using these masks, along with results for a control cell (N+ back area 0%, P+ area 100%). As far as possible, all process steps (silicon, surface finish, diffusions, grid masks, AR coatings) were kept identical for all the CBC and for the control cells. The trends in this table show that when N+ back area reaches 2%, the CBC performance closely approaches that of conventional cells of equivalent thickness and processing. In addition, the series resistance values given in the last column show that there is no serious increase in series resistance until the BSF P+ area falls below 90%.

TABLE 5

TESTS TO DETERMINE TRADEOFF N+ AND P+

BACK SURFACE AREA

N+ Area (%)	P+ Area (%)	Voc (mV)	Jsc (mA/cm^2)	CFF (%)	EFF (%)	R_s (ohm)
10.2	88.5	602	37.3	74	12.3	0.080
5.1	93.6	590	37.9	75	12.5	0.058
2.3	96.4	598	37.7	77	12.9	0.056
0	100	592	37.8	78	12.9	0.055

The edge and back surface N+ layers lead to increased shunting for the cell, as seen by the reduced FF (and often Voc). Separate dark forward diode measurement on this sequence of cells showed that this increased shunting could also be seen on the dark diode characteristics (effective increase in recombination currents at low forward bias voltages), although it was not possible to obtain quantitative agreement between the various dark and illuminated measurements. Nevertheless, these results show that the WAJ design can approach the performance of similarly processed cells without the WAJ structure, provided the N+ area is reduced to ~2%, also further reduction cannot offer suitable increase to justify the additional complexity of mask precision and alignment.

2.3 Choice of Silicon

2.3.1 Resistivity Choice

Even for cells as thin as 50um, it was found that slightly higher electrical performance was obtained if the starting silicon had higher minority carrier diffusion length. Early tests had shown that 10 ohm-cm, back surface field solar

cells would give slightly higher output than cells made from comparable silicon with resistivity around 2 ohm-cm. This resulted from the slightly higher diffusion length for the 10 ohm-cm silicon, leading to higher short circuit current (Isc) and the comparable open circuit voltage (Voc) resulting from an effective BSF; the Isc increase offset the slightly lower CFF for the higher resistivity.

After mid-term technical review with the contract monitor, an additional test was made to fabricate CBC solar cells using 2 ohm-cm, float-zone refined (FZ), material. The results showed that good efficiency of 13.4% could be obtained from 2 ohm-cm silicon, (compared to 13.5% efficiency obtained from 10 ohm-cm silicon). The Isc value for the 2 ohm-cm silicon was only slightly lower, and Voc was slightly higher. However, a small decrease in fill factor (CFF), mainly due to the lower shunting resistance, was observed for 2 ohm-cm silicon. This shunting problem had often been experienced for lower resistivity material processed using any of the BSF formation methods. Because higher resistivity silicon was more reproducible and will also have higher radiation resistance, the preferred resistivity in this work was 10 ohm-cm silicon.

2.3.2 Float-Zone vs Refined Czochralski Silicon

Table 6 gives the comparison of cells made from FZ and CZ grown silicon, using the same process sequence. Noted that the difference in spectral components of Isc showed that most of increased Isc resulted from long wavelength ($> 6000A^{o}$), a clear indication that the slightly higher diffusion length of FZ silicon was responsible for the increase. However, in a practical case, the small difference in output (~3%) can easily be justified either for cost reasons, or to reduce the chance of photon degradation in space operation; thus CZ silicon may be a better choice for practical use.

TABLE 6

CBC CELL PERFORMANCE (FZ SILICON VERSUS CZ SILICON)

	Voc (mV)	Isc (mA)	I_B (mA) ($\lambda > 6000A$)	I_B (mA) ($\lambda < 6000A$)	CFF (%)	EFF (%)	AREA (cm^2)
FZ	598	302.0	175.1	127.4	77	12.9	8.0
CZ	598	296.6	171.6	124.8	76	12.3	8.0

2.4 Solar Absorptance (α_s)

2.4.1 Surface Finish

The contract called for low α_s, which requires that the silicon surfaces be highly polished. However, to show whether the WAJ cell parameters were similar for a textured surface finish, some tests were made using textured FZ silicon with direct comparison with polished slices of the same silicon; both WAJ and control cells were made. The results are shown in Table 7. This direct comparison shows that the textured cells had slightly lower Voc (expected from the increased area of the textured surface) and 4-7% increase in Isc. This Isc increase gave approximately 1% increase in conversion efficiency. These results indicate that if low α_s-values are not required, increased output (up to 15% AMO efficiency) can be obtained for WAJ cells with textured surfaces.

TABLE 7

CHEM-POLISHED VERSUS TEXTURED CELL COMPARISONS

	Voc	Jsc (mA/cm^2)	CFF (%)	EFF (%)
Polished	598	37.7	77	12.9
Textured	597	40.5	76	13.7

2.4.2 Back Surface Reflector

To obtain low αs, the cells not only need to have a highly polished surface, but required a high reflectance metal contact to the silicon on the back.

For this contract, a thin evaporated aluminum layer was used to provide this back surface reflectance, combined with moderate heat treatment to preserve the highly polished surface and contact integrity. The low αs values of 0.73 were obtained for the WAJ cells.

2.5 Back Surface Field (BSF) Formation

With 50um thick cells, it is essential to include an effective BSF, to reduce minority carrier recombination at the nearby back surface. Several methods have been used successfully, including alloying of evaporated aluminum, alloying of screen printed aluminum paste, boron diffusion or boron implantation. Since this contract involved low αs, and the process sequence included many handling steps, we selected boron diffusion for its combination of good surface finish and minimum stress. There are several boron diffusion sources which can be used, but we concentrated on use of boron nitride disks as the boron source. We found that reasonably good BSF performance (some increase in Isc, and in Voc) could usually be obtained, but the uniformity was not as high as required. We tested several different versions of the BN disks, but could not see any consistent dependence on the particular type. The most reproducible results were obtained when great care was taken to ensure good maintenance of the BN disk surface. This BSF method involves higher ($\sim$1000^{o}C) temperatures (and longer times, up to 60 minutes) than the Al alloy method ($\sim$800^{o}C-10 minutes), and there is the added risk of reduced diffusion length under these severe schedules. However, by careful cooling, and ensuring clean slice and tube conditions, we were able to provide acceptably good BSF's while retaining most of the original diffusion length.

Another BSF requirement, specific to the WAJ cells was the need for a method which is compatible with the thin slices, and the precise mask alignment needed to provide accurately located areas of N+ and P+ on the back surface. Again the BN method proved to be satisfactory in this requirement.

At the mid term review, the request was made to explore the evaporated Al-alloy method again, using the complete WAJ cell sequence. The results of this test are shown in Table 8 and indicate that no advantage was seen in this method, using the limited range of alloy BSF formation methods tried.

TABLE 8

CBC CELL PERFORMANCE USING EVAPORATED ALUMINUM ALLOY BSF TECHNIQUE

Voc (mV)	Isc (mA)	CFF (%)	EFF (%)	AREA (cm^2)
527	280.0	75.0	10.1	8.0

We mentioned above that most of the BSF methods used, led to increased shunting when combined with low resistivity silicon, and this has not been completely explained, although in severe cases, front N+ surface contamination by the acceptor could be detected. Thus, generally thin cells with BSF gave increased shunting when 2 ohm-cm rather than 10 ohm-cm silicon was used. To illustrate the best performances observed for 2 ohm-cm silicon (although with less consistency than with the higher resistivity), an additional group processed in the final run using 2 ohm-cm silicon, is described below in Section 2.8.

2.6 Simulator Calibration

Early in the contract, a comparison was made (on the same group of CBC cells) of measurements taken on ASEC's AMO simulator and AMO measurements at NASA-Lewis Research Center. This comparison is shown in Table 9. These measurements show close agreement both in light source calibration, and in the special fixturing used to test CBC cells.

2.7 Chronological Performance

Table 10 shows the I-V performance of the best cells delivered at regular intervals during the contract. The table also shows the performance of 50um thick control cells fabricated in similar fashion to the CBC cells. Based on the tests performed in the first nine months, the process sequence shown to be optimum, was used to fabricate the fifty deliverable cells.

2.8 Final Deliverable Cells

2.8.1 Fabrication

During the first eight months we had identified the key process steps and design parameters for the fabrication of efficient 2 mil, WAJ solar cells. The resultant WAJ cells reached an AMO efficiency of 13.6% at 25°C. A proposed baseline process sequence was sent to NASA-Lewis Research Center for approval for the final pilot run. Upon approval by the contract monitor, material and process traveler forms were prepared such that each step was traceable and properly executed. The process loss and yield were also recorded in the travel sheet.

As requested in the contract, three separate equal size lots, each consisting of fifty (50) 3" diameter wafers were processed in accordance with the baseline cell process reference as shown in Table 11. The base material was 10 ohm-cm, p-type,

TABLE 9

SIMULATOR CALIBRATION

	Voc (mV)		Isc (mA)		CFF (%)		EFF (%)	
	NASA LeRC	ASEC	NASA LeRC	ASEC	NASA LeRC	ASEC	NASA* LeRC	ASEC
1	595	591	153.8	154.5	77.5	78	12.93	13.1
2	594	590	154.7	155.	76.9	77	12.89	13.0
3	598	591	155.9	156.1	76.3	77	12.99	13.08
4	593	598	152.5	153.7	76.4	77	12.62	13.1
5	596	593	152.5	153.7	77.0	77	12.76	13.0
6	594	590	154.4	154.8	76.7	77.4	12.85	13.05
7	594	592	153.4	154.2	76.2	76.5	12.68	13.0
8	594	589	153.3	153.3	77.2	77	12.83	12.9

*Pin = 137.5 mW

TABLE 10
CHRONOLOGICAL PERFORMANCE, 2x4cm CELLS

DELIVERY DATE		AMO*					COMMENTS 0
		Jsc	Voc	FF	EFF	BACK AREA N+ %	
		mA/cm^2	mV	%	%		
November 1980		35.9	606	0.75	12	10	CZ Si
December 1980		35.3	610	0.76	12.1	10	CZ Si
January 1981		24.1	484	0.77	7.1	10	CZ Si, High Temp. Oxidation Cycle
	Control	25.6	472	0.76		0	FZ
February 1981		37.3	602	0.74	12.3	10	FZ
		37.9	590	0.75	12.5	5	FZ
	Control	37.6	579	0.77	12.2	0	FZ
		36.1	583	0.74	11.6	10	CZ
		35.8	583	0.75	11.7	5	CZ
	Control	35.8	576	0.78	11.9	0	CZ
March 1981		37.8	598	0.77	12.9	2	FZ
	Control	37.8	592	0.78	12.9	0	FZ
		40.6	597	0.76	13.7	2	FZ,Textured
	Control	39.5	588	0.77	13.3	0	FZ,Textured
		37.1	598	0.75	12.3	2	CZ
	Control	36.8	590	0.77	12.4	0	CZ
April 1981		36.9	592	0.75	12.2	2	FZ-Different BSF
	Control	37.2	593	0.77	12.6	0	FZ Schedule
		39.8	593	0.76	13.4	2	FZ,Textured
	Control	39.8	593	0.75	13.1	0	FZ,Textured
May 1981	Control	39.4	615	0.77	13.8	0	CZ, Improved BSF
June 1981		35.0	527	0.74	10.1	2	CZ,Al BSF
July 1981		39.1	618	0.75	13.4	2	FZ, 2 ohm-cm
	Control	38.4	616	0.77	13.5	0	FZ, 2 ohm-cm

*135.5 mW/cm^2, Cell Temperature 25°C.

0 Unless noted, cells have coplanar back contacts and silicon resistivity - 10 ohm-cm.

TABLE 11

BASELINE PROCESS SEQUENCE

STEP NO.	STEP
1	Wafer Preparation (50um)
2	SiO_2 Deposition (CVD + Thermal Oxidation)
3	Open Window For BSF Formation
4	Boron Diffusion (BSF)
5	SiO_2 Deposition (CVD)
6	Open Window For Wraparound Edge Diffusion
7	N+ Diffusion
8	Open Front Surface
9	N+ Diffusion
10	Front Contact Formation
11	Trim To Size
12	Back Contact Formation
13	AR Coating
14	Sinter
15	Test

TABLE 12 (a), 10 ohm-cm

UNIT	V_{oc}	I_{sc}	I_L (at 0.5V)	P (at 0.5V)	CFF	EFF AT 0.5V
	mV	mA	mA	mW		%
1	604	314.1	287.6	143.8	$.75_8$	13.3
2	610	302.0	284.6	142.3	$.77_2$	13.1
3	613	318	284	142	$.72_8$	13.1
4	602	307.0	278.0	139	$.75_2$	12.8
5	602	314.2	282.0	141	$.74_5$	13.0
6	600	312.3	273.4	136.7	$.72_9$	12.6
7	608	312.5	290.4	145.2	$.76_4$	13.4
8	608	318.0	290.5	145.3	$.75_1$	13.4
9	610	311.2	292.0	146	$.76_9$	13.5
10	598	309.0	284.5	142.3	.77	13.1
11	607	317.0	281.5	140.8	$.73_1$	13.0
12	599	303.0	274.4	137.2	$.75_6$	12.7
13	606	307.0	285.0	142.5	$.76_6$	13.2
14	610	311.0	286.3	143.2	$.75_5$	13.2
15	610	306.0	287.0	143.5	$.76_9$	13.3
16	601	305.5	268.1	134.1	.73	12.4
17	604	307.1	271.0	135.5	$.73_1$	12.5
18	602	312.3	284.0	142	$.75_5$	13.1
19	606	303.3	274.5	137.3	$.74_7$	12.7
20	611	308.9	287.4	143.7	$.76_1$	13.3
21	594	311.9	274.2	137.1	.74	12.7
22	606	308.3	283.3	141.7	$.75_8$	13.1
23	606	303.9	283.0	141.5	$.76_8$	13.1
24	609	309.0	285.5	142.8	$.75_9$	13.2
25	602	316.0	275.3	137.7	$.72_4$	12.7

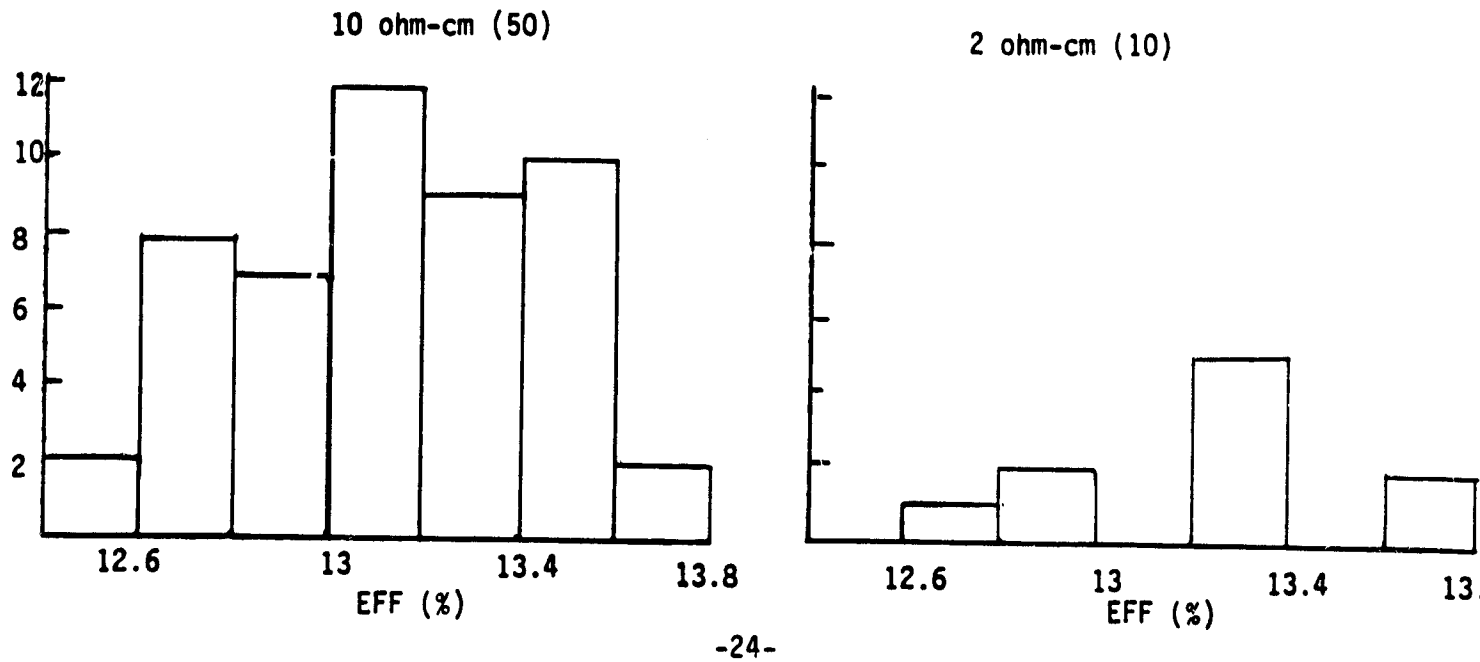
TABLE 12 (a), 10 ohm-cm Cont'd.

UNIT	V_{oc}	I_{sc}	I_L (at 0.5V)	P (at 0.5V)	CFF	EFF AT 0.5V
	mV	mA	mA	mW		%
26	598	308.5	276.5	138.3	$.74_9$	12.8
27	615	313.1	292.0	146	$.75_8$	13.5
28	611	304.4	278.0	139	$.74_7$	12.8
29	613	316.0	283.0	141.5	.73	13.1
30	615	312.0	292.0	146	$.76_1$	13.5
31	610	313.1	290.7	145.4	$.76_1$	13.4
32	610	313.2	290.0	145	$.75_9$	13.4
33	603	313.9	282.3	141.2	$.74_6$	13.0
34	614	313.4	290.5	145.3	$.75_5$	13.4
35	605	311.9	276.7	138.4	$.73_3$	12.8
36	611	309.1	287.3	143.7	$.76_1$	13.3
37	608	315.0	288.0	144	$.75_2$	13.3
38	604	315.0	280.2	140.1	$.73_6$	12.9
39	610	312.1	282.7	141.4	$.74_2$	13.1
40	605	312.7	280.1	140.1	.74	12.9
41	609	302.8	273.0	136.5	.74	12.6
42	599	312.0	275.7	137.9	$.73_8$	12.7
43	614	310.2	274.0	137	$.73_1$	12.7
44	604	310.0	282.0	141	$.75_3$	13.0
45	611	311.0	288.1	144.1	$.75_8$	13.3
46	611	300.1	277.2	138.6	$.75_6$	12.8
47	615	311.5	292.0	146	$.76_2$	13.5
48	612	316.5	293.0	146.5	$.75_6$	13.5
49	612	313.2	294.0	147	$.76_7$	13.6
50	615	314.6	297.0	148.5	$.76_3$	13.7

TABLE 12 (a), 2 ohm-cm

UNIT	V_{oc}	I_{sc}	I_L (at 0.5V)	P (at 0.5V)	CFF	EFF AT 0.5V
	mV	mA	mA	mW		%
51	617	310.2	297.5	148.8	$.77_7$	13.7
52	604	301.3	276.1	138.1	$.75_9$	12.8
53	600	310.2	285.7	142.9	$.76_8$	13.2
54	610	303.9	288.5	144.3	$.77_8$	13.3
55	610	310.2	287.0	143.5	$.75_8$	13.3
56	606	293.1	277.3	138.7	$.78_1$	12.8
57	612	305.0	294.0	147	$.78_8$	13.6
58	608	302.8	289.0	144.5	$.78_5$	13.3
59	609	306.5	286.0	143	$.76_6$	13.2
60	589	299.6	275.4	137.7	.78	12.7

FIGURE 2 - HIRTOGRAM PLOT



FZ silicon of (100) orientation for Lot I and Lot II, while the Lot III was 2 ohm-cm with similar crystal quality. This is because we felt that fabrication of cells from both resistivities would provide the chance of direct comparison in radiation tolerance, and would show increased possibilities to attain the contract goals.

In order to reach the upper contract goal of 14%, in the short time remaining on the contract, the cell processing steps and parameters (Voc, Isc, CFF) were evaluated and analyzed. We concluded that a better controlled AR coating would improve Isc slightly and would possibly result in reaching the 14% AMO goal.

2.8.2 Electrical Performance

Cell electrical output was measured using a Xenon-tungsten light simulator calibrated by reference cells tested by NASA-Lewis (see 2.6). All measurements were taken under AMO (135.3 mW/cm^2) illumination at 25^{o}C. A total of sixty CBC cells were tested and delivered to NASA-Lewis, 50 cells using 10 ohm-cm silicon, and 10 cells using 2 ohm-cm silicon. The digital readout and power distribution for these cells are given in Table 12 (a)-(b) and Figure 2. The I-V curves for the best WAJ cell (14.1%) are shown in Figure 3.

2.8.3 Process Loss and Yield Summary

Table 13 shows the process loss and yield at each process step for all three lots of the final pilot run. The mechanical criteria used were similar to those used in the space cell manufacturing industry. The minimum electrical output was set at 12%.

FIGURE 3

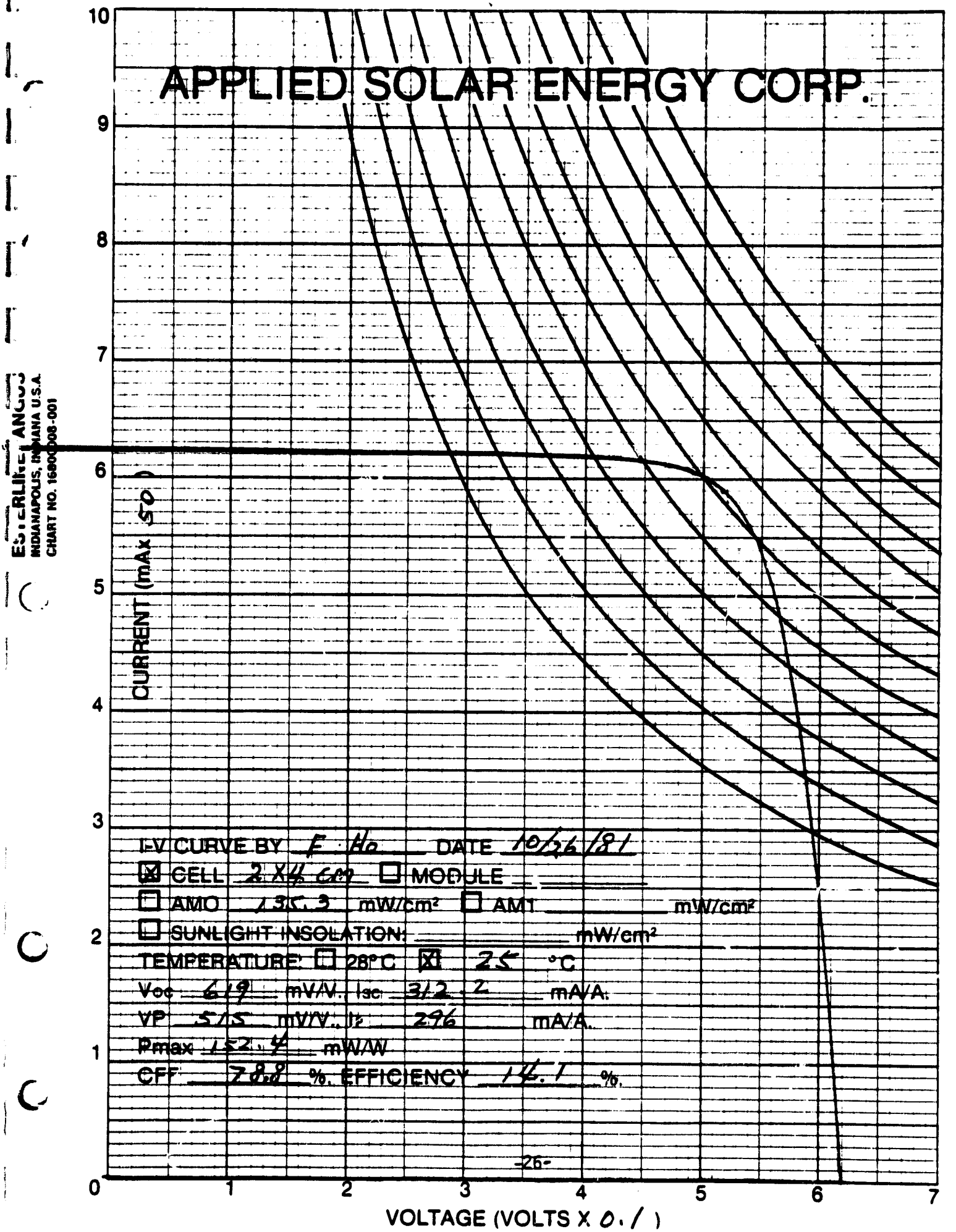


TABLE 13

PROCESS LOSS AND YIELD SUMMARY FOR THE THREE FINAL PILOT RUNS

PROCESS LOSS AND REJECT MODE	LOT NUMBER I (%)	II (%)	III (%)
Cleaning and Etching	10.2	12	10.7
SiO_2 Deposition	2	2.5	3.5
Diffusion ($POCl_3$, BN)	6	5.5	2
Photoresist Work	12.8	3.5	8.7
Metallization	4	6	6
Plating	6.4	8	8.5
Cutting and AR Coating	0.6	0.5	1.3
Mechanical Reject	6.7	8	18
Electrical Reject ($<$ 12% AMO)	14	12.7	7.3
TOTAL YIELD ($\geq$ 12%)	37.3	41.3	34

2.8.4 **Environmental Tests**

a) Contact Adhesion

Early tests showed that both N+ and P+ area contacts had pull strengths above 600gm.

b) Contact and Coating Adherence Test

Six cells were selected at random from each lot for tape test. Cells were tested and mounted on a thick silicon slice using wax, three cells for front contact test, and the other three cells for back contact test. All the cells were then passed through a machine which applied and peeled scotch 610 tape to the contact. After this test, three cells were found broken, and the good

cells show less than 3% of the grid contact removed by this tape test. The differences in cell performance and after tape test are given in Table 14.

TABLE 14

TEST BEFORE TAPE TEST

	Voc (mV)	Isc (mA)	CFF (%) (at 500mV)	EFF (%) (at 500mV)
1.	584	307	73.0	12.1
2.	605	299	78.0	13.0
3.	588	310.7	73.0	12.3
4.	584	310.7	68.0	11.4
5.	563	298.0	68.0	10.5
6.	584	302.0	67.0	11.0

TEST AFTER TAPE TEST

	Voc (mV)	Isc (mA)	CFF (%) (at 500mV)	EFF (%) (at 500mV)
1	———	CELL BROKEN	———	———
2	603	300.0	77.0	12.9
3	589	311.0	73.0	12.3
4	———	CELL BROKEN	———	———
5	———	CELL BROKEN	———	———
6	585	301.7	68.0	11.0

c) Temperature/Humidity Test

Three cells, one cell from each lot, were selected and tested for electrical output and then subjected to 30 days of continuous storage in a chamber at 45°C and 90% relative humidity. After the humidity test the cells were again

tested, and the changes in cell performance was noted. It was observed that the cell degraded only 0.4% in efficiency. (See Table 15)

TABLE 15

TEST BEFORE HUMIDITY CYCLE

	Voc (mV)	Isc (mA)	CFF (%)	EFF (%) At 500 mV
1.	610	304.1	75	12.9
2.	594	313.1	73	12.5
3.	608	309.2	76	13.2

TEST AFTER HUMIDITY CYCLE

	Voc (mV)	Isc (mA)	CFF (%)	EFF (%) At 500 mV
1.	602	303.2	74	12.5
2.	589	311.4	71	12.1
3.	602	308.2	75	12.8

c) Thermal Shock Test

Three cells, one cell from each lot, were selected for thermal shock test. All the cells were put into a chamber for 10 temperature cycles between -196°C and 100°C with 2 minutes dwell time at each temperature extreme. The elctrical performance was measured before and after cycling. There was no indication of any degradation caused by this test. (See Table 16)

TABLE 16

BEFORE THERMAL SHOCK CYCLE

	Voc (mV)	Isc (mA)	CFF (%)	EFF (%)
1.	610	305.2	76	13.0
2.	586	300.5	75	12.3
3.	613	314.5	74	13.1

AFTER THERMAL SHOCK CYCLE

	Voc (mV)	Isc (mA)	CFF (%)	EFF (%)
1.	610	305.0	75	12.9
2.	587	299.8	75	12.3
3.	612	314.4	74	13.1

2.9 Theoretical Model

Most of the cell analysis could be fitted to conventional cell models. For CBC cells with WAJ structure, this similarity extended to the effects of the reduced P+ BSF area on the back surface. When the BSF layer was not present on parts of the back cell surface, reduced Jsc and some loss of Voc were expected and observed.

In addition, there was some slight increase in series resistance caused by the larger path length for carriers generated away from the area with contact to the BSF layer; generally these P+ area losses were minimized by reducing the area of the N+ back surface area, and by increasing the P+ contact area. This can be seen from the results given in Table 5, where the best WAJ cells had performance approaching that of similarly processed control cells which have full P+ area contacts.

One area which does not fit conventional theory is that involving the increased shunting (with reduced CFF and increased dark diode leakage current at low voltages) observed for N+ back areas above 3%. This same effect led to the results observed (varying CFF, total Jsc not equal to separate spectral components) when WAJ cells were illuminated non-homogeneously, i.e. at the WAJ ends only, or over the whole cell, including the WAJ ends.

With cooperation from C. Baraona (NASA-Lewis Research) and C. Goradia (Cleveland State University) tests were made a computer model, developed for interdigitated back contact cells, to explain the effects. Unfortunately, this model did not explain or predict the type of shunting behavior observed.

Although the empirical approach described above was successful in leading to efficient WAJ cells, it would be satisfying to have evolved a theoretical model which explained the success of the empirical work.

3.0 CONCLUSIONS AND RECOMMENDATIONS

The contract program described above showed that by careful application of current 50um cell technology and optimization of a sequence which gave a minimum N+ area WAJ structure, CBC cells could be consistently fabricated which met the contract goals. This list of achieved goals is as follows:

- 50um CBC cells, 8cm^2 were fabricated.
- The cells shipped exceeded the minimum goal (12%).
- The average efficiency was ~13% for the lowαs cells.
- The maximum goal (14%) was achieved.
- The process sequence was moderately compiex, but showed good reproducibility.
- The yield obtained (overall ~35-40%) was comparable to that seen for similar area conventional cells of the same thickness.
- The CBC cells performed well under several important environmental tests.
- If high αs cells can be used to advantage, ~1% increase in conversion efficiency can be obtained.

This extension of 50um cell performance to include coplanar back contacts is useful as an option for array designers, who may be able to exploit the CBC structure to reduce costs or increase the effectiveness of thin cell array assembly.

The work has shown that further improvements should be obtainable. These improvements include:

- Extension to larger areas (up to 25cm^2 or larger). The main problem which can be foreseen is the chance of reduced yield (same problem with conventional thin cells).
- Inclusion of other thin cell advantages (ultra lightweight, reduced bowing).

- Proof that CBC thin cells have advantages in array interconnection and/or in glassing (probably best done by array manufacturers).
- Development of a suitable theoretical model for WAJ structure.
- Direct comparison with wrap-around dielectric contact structure.
- Extension of WAJ structure to thicker cells, to see if this structure has CBC advantages.
- Further development of CBC thin cell processes which can reduce complexity, reduce costs and increase yields.

In conclusion, the cells produced under this contract represent a step forward in thin cell technology.

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